FET NOISE MODEL AND ON-WAFER MEASUREMENT OF NOISE PARAMETERS

Marian W. Pospieszalski
National Radio Astronomy Observatory*
Charlottesville, Virginia 22903

Antoni C. Niedzwiecki
Avantek, Inc.
Santa Clara, California 95054

ABSTRACT

The recently published noise model of a microwave FET [1], [2] is verified for the first time with on-wafer S-parameters and noise parameters measurement data. An excellent agreement between the model prediction and measurement results is obtained for a wide range of FET bias. It is shown that the equivalent drain temperature is a very strong function of the drain current, while the equivalent gate temperature is a very weak function of the drain current and, within the measurement error, it is equal to the ambient temperature for small drain currents.

INTRODUCTION

The recently published noise model of a FET (MODFET) [1], [2] postulates that four noise parameters of the transistor can be determined at any frequency at which 1/f noise is negligible by the knowledge of the transistor equivalent circuit and two frequency independent constants T_g and T_d, named gate and drain equivalent temperatures, respectively. The drawback of previous verifications [1]-[4] was that the noise parameter data and S-parameter data were taken for different samples of the same type device at a single operating bias. This paper presents for the first time the verification of the model with on-wafer noise parameters and S-parameters data for a number of transistors as a function of operating bias.

Noise Parameters and S-Parameters Measurement

Noise and S-parameter measurements were taken with a Cascade Microtech wafer probe and on-wafer noise parameter measurement system [5]. S-parameters were measured in the 1-26 GHz range using LRM calibration. Noise parameters were measured in the 2 to 18 GHz range. Several FET's with the gate dimensions .3 x 250 μm were tested for drain voltages V_{ds} = 2-3 V and drain currents I_{ds} = 10-90 mA. For each operating bias, the equivalent circuit of a FET was determined using GaAs Code software [6]. A typical equivalent circuit of a FET is shown in Figure 1. The gate and source parasitic resistances were fixed at $r_g = 1.0\ \Omega$ and $r_s = .7\ \Omega$, respectively, while intrinsic gate resistance r_{gs} was determined in the fitting procedure. The example of the dependence of intrinsic gate resistance r_{gs} and drain resistance r_{ds} on FET bias is shown in Figures 2 and 3, respectively.

Noise Model and Measured Noise Parameters

The measured noise parameters given in the form F_{min}, Γ_{opt} and R_n were converted first into T_{min}, R_{opt}, X_{opt} and g_n. For the model, this set of noise parameters in the case of intrinsic chip and small signal approximation is given by [1], [2]:

$$T_{min} \simeq 2\frac{f}{f_T}\sqrt{g_{ds}\, r_{gs}\, T_g\, T_d} \qquad (1)$$

$$R_{opt} \simeq \frac{f_T}{f}\sqrt{\frac{r_{gs}}{g_{ds}}\frac{T_g}{T_d}} \qquad (2)$$

$$X_{opt} = \frac{1}{\omega\, C_{gs}} \qquad (3)$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds}\, T_d}{T_o} \qquad (4)$$

where $f_T = g_m/2\pi\, C_{gs}$, T_o = 290 K, $g_{ds} = 1/r_{gs}$. It is clear from (1) through (4) that in order to find the equivalent gate and drain temperatures, it is enough to consider only the fit for R_{opt} and T_{min}. A typical set of measured unsmoothed data and the model fit for four drain currents of a sample device is shown in Figure 4. The temperature of parasitic elements r_g, r_s and r_d was assumed to be T_a = 297 K. Only measured and model-computed data for R_{opt} and T_{min} in the frequency range 4-18 GHz were fitted in the mean square sense to arrive at values of T_g and T_d for each bias. Thus, the agreement between measured and computed values of X_{opt} and g_n serves only as a check of the model's consistency. The agreement is indeed very good within the frequency range 3 to 18 GHz. For most of the transistors,

*The National Radio Astronomy Observatory is operated by Associated Universities, Inc. under cooperative agreement with the National Science Foundation.

JJ

CH2870-4/91/0000-1117$01.00 © 1991 IEEE

there is a discrepancy between measured and predicted values of noise parameters at 2 GHz. This could be partially accounted for by making the gate temperature frequency dependent (1/f noise). However, for the measurement data to be interpretable by the model (with or without frequency dependence of T_d and T_g), the following inequality has to be satisfied:

$$1 \le \frac{4N\,T_o}{T_{min}} < 2 \tag{5}$$

All of the data at 2 GHz violate the righthand side of this inequality, suggesting the presence of a systematic measurement error.

The dependence of equivalent drain and gate temperatures on drain current is shown in Figure 5, and the expanded plot for gate temperature is shown in Figure 6. The data taken for three devices are plotted on the same graph. The equivalent drain temperature is strongly dependent on the drain current and, within the measurement error, a single function may describe its dependence for all devices. The equivalent gate temperature is a very weak function of drain current and for low-noise bias ($I_{ds} \approx 10$ mA) is equal within measurement error to the ambient temperature of the device. The approximately linear dependence of gate temperature on drain current can probably be explained by thermal effects only. The scatter in the values of the equivalent gate temperatures (compare Figure 5) may be explained by the error in determination of the intrinsic gate resistance r_{gs} and parasitic resistances r_g and r_s. The dependence of minimum noise temperature on drain current is shown in Figure 7. This dependence can be explained by the corresponding changes in f_T and T_d, also shown in Figure 7 (compare equation (1)).

CONCLUSIONS

The analysis of on-wafer measurement of noise parameters strongly supports the validity of the noise model introduced in [1], [2]. There is no evidence of correlation between noise processes represented by equivalent temperatures T_g and T_d. That is, for the intrinsic chip, the noise observed at the source-drain terminals under open-circuited gate does not induce any noise in the gate circuit. This is in disagreement with the usual treatment of gate noise in FET's (for instance, [7]-[9]). A single frequency noise parameters measurement (at least T_{min} and R_{opt}) is sufficient to determine the noise performance of a FET for its useful frequency range if the device equivalent circuit is known. An optimal operating bias for a given transistor is the one minimizing the value of

$$f(V_{ds}, I_{ds}) = \frac{\sqrt{T_d\, g_{ds}}}{f_T} \tag{6}$$

The same parameter should be considered in the search for new device structures for low-noise applications.

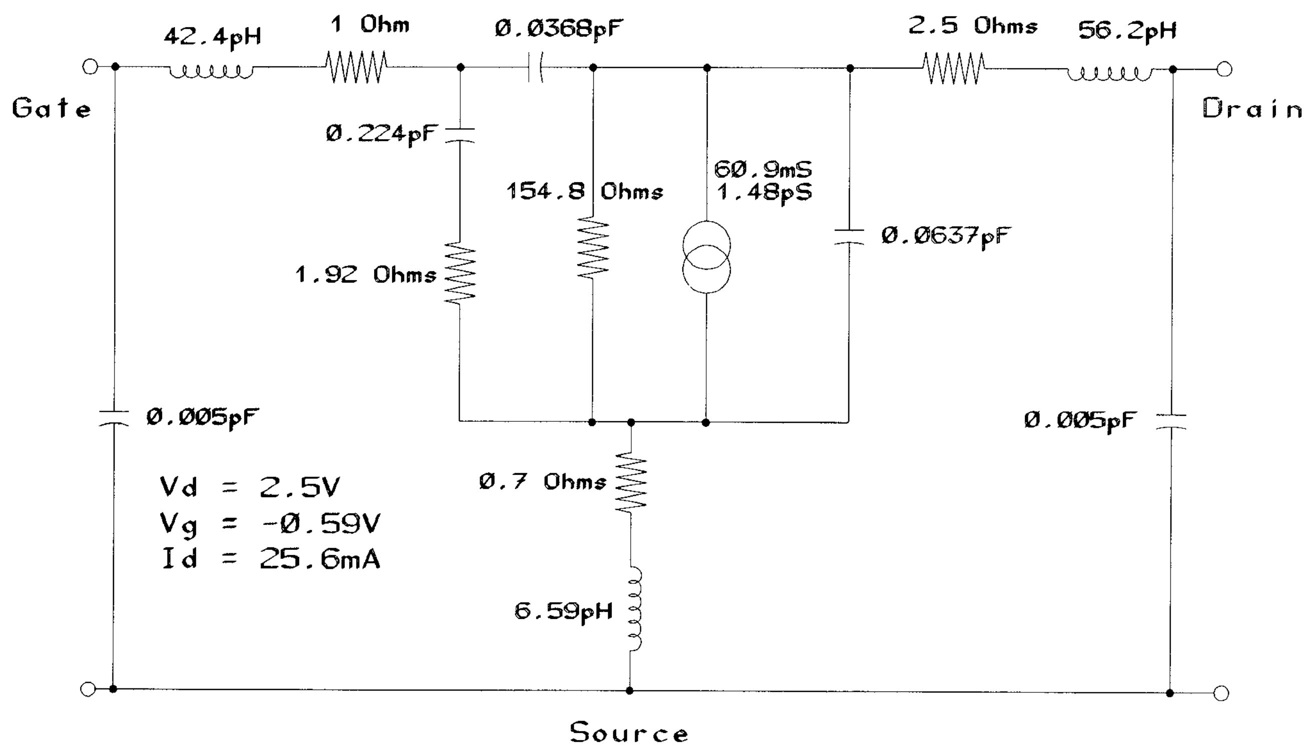

Fig. 1. An example of the equivalent circuit of a FET under investigation.

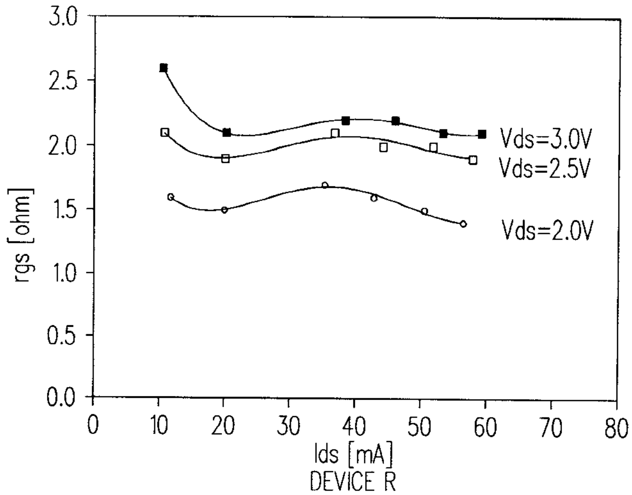

Fig. 2. An example of bias dependence of the intrinsic gate resistance r_{gs}.

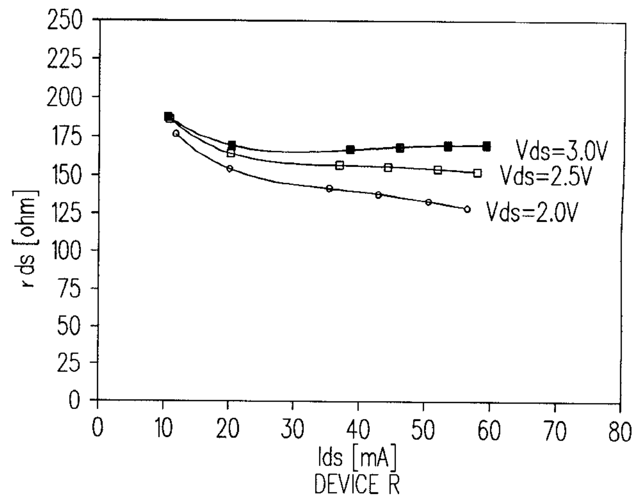

Fig. 3. An example of bias dependence of the drain resistance r_{ds}.

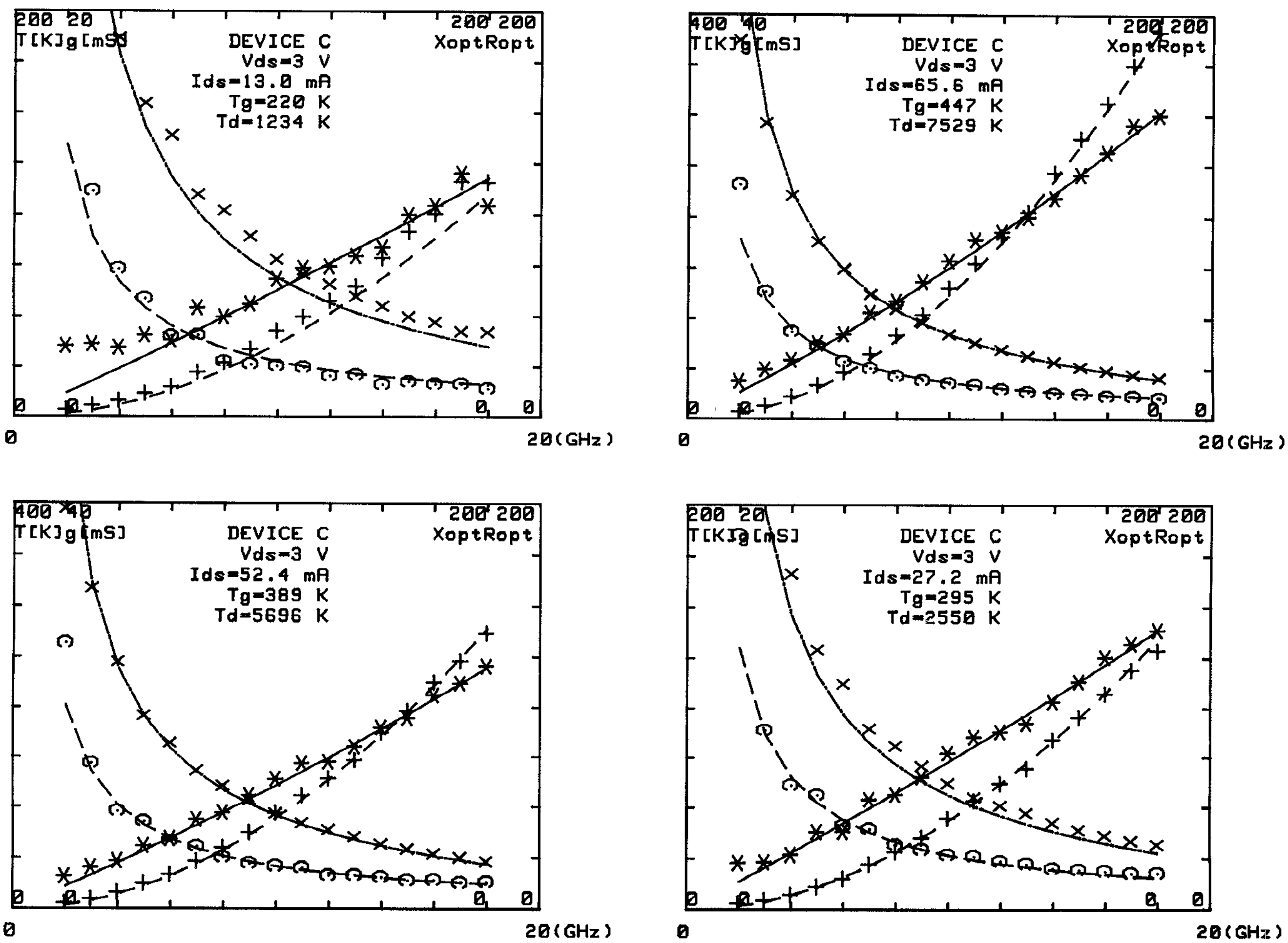

Fig. 4. Examples of measured and model-predicted noise parameters of a sample device (C) for different bias currents. Measured values given by symbols: "*" for T_{min}, "O" for R_{opt}, "X" for X_{opt} and "+" for g_n. Model-predicted values given by lines.

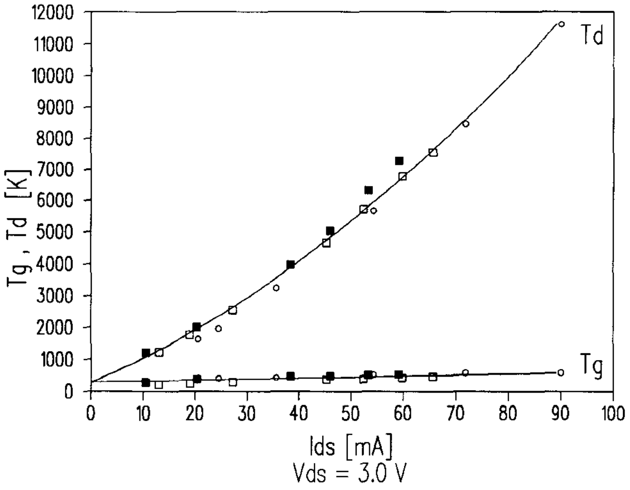

Fig. 5. Equivalent gate and drain temperatures vs. drain current (data plotted for three devices B "o", C "□" and R "■").

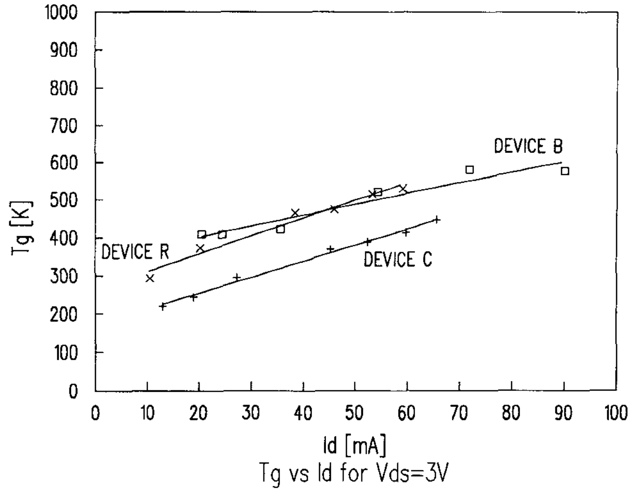

Fig. 6. Equivalent gate temperature vs. drain current (data plotted for three devices B, C and R).

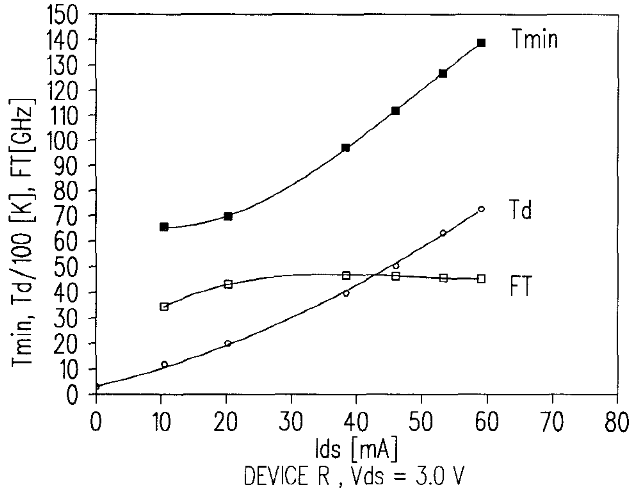

Fig. 7. Minimum noise temperature T_{min}, equivalent gate temperature T_d and intrinsic cut-off frequency f_T as a function of drain current.

REFERENCES

[1] M. W. Pospieszalski, "A New Approach to Modeling of Noise Parameters of FET's and MODFET's and Their Frequency and Temperature Dependence," NRAO Electronics Division Internal Report No. 279, Charlottesville, VA, July 1988.

[2] M. W. Pospieszalski, "Modeling of Noise Parameters of MESFET's and MODFET's and Their Frequency and Temperature Dependence," *IEEE Trans. on MTT*, vol. MTT-37, pp. 1340-1350, September 1989. (Also in *Proc. 1989 Int. Microwave Symp.*, pp. 385-388, Long Beach, CA, June 1989.)

[3] M. W. Pospieszalski, J. D. Gallego, and W. J. Lakatosh, "Broadband, Low-Noise, Cryogenically-Coolable Amplifiers in 1 to 40 GHz Range," in *Proc. 1990 MTT-S Int. Microwave Symp.*, pp. 1253-1256, Dallas, TX, May 1990.

[4] J. D. Gallego and M. W. Pospieszalski, "Design and Performance of Cryogenically-Coolable, Ultra Low-Noise, L-Band Amplifier," in *Proc. 20th European Microwave Conf.*, Budapest, Hungary, pp. 1755-1760, September 1990.

[5] Cascade Microtech, Inc., 14255 SW Brigadoon, Beaverton, OR 97005.

[6] GaAs Code, Ltd., St. John's Innovation Centre, Cowley Road, Cambridge CB4 4WS, England.

[7] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and Noise Properties of GaAs Microwave FET," in *Advances in Electronics and Electron Physics*, vol. 38, L. Morton, ed., NY: Academic Press, 1975.

[8] A. Cappy, "Noise Modeling and Measurement Technique," *IEEE Trans. on MTT.*, vol. 36, pp. 1-10, January 1988.

[9] K. Joshin, *et al.*, "Experimental and Theoretical Noise Analysis of Microwave HEMT's," *IEEE Trans. on Electron Devices*, vol. ED-36, pp. 2274-2280, October 1989.